Dual Role CDSC based Dual Vector Control for Effective Operation of DVR with Harmonic Mitigation

A. Karthikeyan, *IEEE Member*, D.G. Abhilash Krishna, *Student Member*, Sushant Kumar, B. Venkatesa Perumal, *IEEE Member*, and S. Mishra, *Senior Member*

Abstract— **For the effective operation of Dynamic Voltage Restorer (DVR) control strategy plays significant role. This paper presents enhanced control strategy for DVR using dual role Cascaded Delay Signal Cancellation (CDSC) based Dual Vector Control (DVC) under unbalanced and distorted grid conditions. Based on the numerical analysis it is found that CDSC prefilter is promising solution when grid voltage is distorted by symmetric, asymmetric harmonics and unbalanced sag. Mainly, CDSC prefilter extracts Instantaneous Symmetrical Components (ISC) of the grid voltage required for voltage sags detection and generation of fundamental component of reference voltage for the DVR. A CDSC based DVC algorithm with inductor current and capacitor voltage feedback is implemented in synchronous reference frame, which tracks the fundamental DVR reference voltages. An extractor based on modified CDSC strategy is designed to extract harmonics from load voltage during distorted grid conditions. These extracted harmonic components (non-fundamental) are added in phase opposition with fundamental component and fed to PWM block to generate reference voltages. Experimental studies are conducted on scaled down (100 V, 0.5 kVA) laboratory prototype DVR to verify the effectiveness of the proposed control algorithm under unbalanced and distorted grid conditions.**

Keywords—CDSC; Extractor; Pre-filter; Symmetric and asymmetric voltage sags, harmonics; Medium Voltage DVR; Double Vector Control;

I. INTRODUCTION

POWER Quality (PQ) has become a serious concern with deregulation of energy markets and increased use of power electronics based loads. These types of loads are nonlinear in nature and its abundant usage results in injection of harmonics into the system thereby decline quality of power. To address these power quality issues viz., voltage sags, swell and harmonics Dynamic Voltage Restorer (DVR) has been proposed [1], [2] as shown in Fig.1. For effective utilization of DVR, two major aspects play significant role: reference generation and control.

Manuscript received December 21, 2017; revised February 2, 2018; accepted April 2, 2018. This work was supported by the administration of National Institute of Technology Karnataka, Surathkal and the Department of Science and Technology, India, under project Grant (SB/FTB/ETA-0020/2014).

A. Karthikeyan, D.G.Abhilash Krishna, Sushant Kumar and B. Venkatesa Perumal are with the EEE Department, National Institute of Technology Karnataka, Mangalore, Karnataka, India .
S. Mishra is with the Indian Institute of Technology Delhi, Delhi, India.
(corresponding author e-mail: jakarthik@nitk.edu.in).

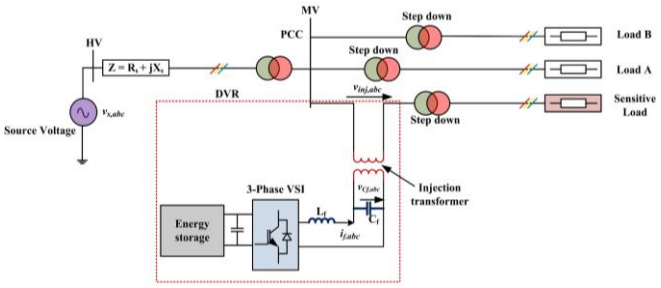

Fig.1 Dynamic Voltage Restorer

Reference generation algorithms based on synchronous reference frame theory usually employ Synchronous Reference Frame (SRF) -Phase Locked Loop (PLL) for this purpose. The presence of negative sequence components and harmonics in grid voltage leads to sustained oscillations in the *dq*- voltages computed by a conventional SRF-PLL. PLLs are proposed in literature with different in-loop and pre-filtering techniques to eliminate these oscillations. However for DVR application Moving Average Filter (MAF)-PLL[4], Delayed Signal Cancellation (DSC)-PLL [5], Least Error Squares (LES) filter based PLL [6], [7] are proposed for extraction of ISC of the grid voltage. Even though MAF-PLL eliminates all even and odd order harmonics it takes one cycle to block these harmonics[8]. The complexity of LES-PLL increases with the number of harmonics present in the grid voltage. DSC-PLL proposed in the literature is not effective when the grid voltage contains asymmetric odd order harmonics (+5, -7...), even though it can filter the fundamental negative sequence voltages and symmetric odd order harmonics (-5, +7…). Hence the *dq*-voltages of the grid v_{dq} estimated by DSC-PLL contains an oscillating component which makes it difficult to enable and disable DVR. Double Second Order Generalized Integrator (DSOGI) -PLL [9] can filter out these harmonics but it offers a tradeoff between speed and its filtering ability. CDSC-PLL extends the concept of DSC by cascading multiple delay operators to eliminate both asymmetric odd and even order harmonics[10]–[12]. Unlike other filters, CDSC filter can be customized by cascading different delay operators to eliminate specific group of harmonics and thus offers flexibility to eliminate harmonics of interest without effecting (compromising its dynamic response) its speed [14]. Also CDSC operator can be placed as either pre-filter or in-loop filter. In this paper $CDSC_{4,\ 8,\ 16,\ 32}$ pre-filter is implemented by cascading multiple delay operators DSC_4, DSC_8, DSC_{16}, DSC_{32} to eliminate symmetric and asymmetric odd harmonics and separate the ISC of the grid voltage. In order to inject desired

compensating voltage, the DVR should be operated by using a proper control strategy.

Several control methods have been proposed in literature for the control of DVR [13] - [26]. Multiple reference frame [23] based controllers with resonant filter, Improved SRF controller with high-pass filter for harmonic elimination [24] are also proposed in literature, but these algorithms are complex as they involve multiple reference frame transformations. Double Vector Control algorithm with resonant controllers [25] is proposed in literature to improve the transient response of DVR and eliminate harmonics from load voltage respectively. Though this scheme was tested for voltage harmonics, but for unbalanced voltage sags the validation of this scheme is not shown. Modified Double vector Control is proposed in [5] to compensate for both balanced and unbalanced dips. Even though, the grid voltage distortions were considered previously in literature, no clear classification of symmetric and asymmetric voltage harmonics is defined, and no separate tests were carried out. These symmetric and asymmetric voltage harmonics becomes relevant if there is spike in the grid connected single phase non-linear loads. In this paper, a dual role CDSC based DVC is presented for DVR control and harmonics mitigation. The compensation voltage injected by DVR includes both fundamental and non-fundamental component. The proposed dual role CDSC has a feature of generating both components simultaneously. Firstly, the prefilter extracts ISC of grid voltage and given to controller to generate fundamental component. Apart from that to achieve the harmonic mitigation of load voltages an extractor based on modified CDSC strategy is designed which generates non-fundamental component of compensation voltage and added in 180^0 phase opposition to the DVC algorithm. Thereby this paper eliminates the use of additional controllers for harmonic compensation such as resonant controllers proposed in the literature, because the single CDSC operator is performing the dual role as pre-filter and extractor. In this application, many authors have addressed the harmonic compensation during unbalanced grid conditions but here an attempt is made to classify harmonics into symmetric, asymmetric and its compensation is achieved during distorted grid conditions.

The paper is organized as follows. The section two starts with the brief introduction of various harmonics that occur in grid voltage. Then the role of CDSC as pre-filter and extractor are explained with respective mathematical equations and the frequency response of CDSC-PLL, DSOGI-PLL, DSC-PLL and SRF-PLL under distorted grid conditions is studied. In section III the proposed CDSC based DVC control scheme is discussed. In section-IV the EMTDC/PSCAD simulation results of medium voltage DVR for asymmetric and symmetric harmonics cases are presented. In section-V experimental results of proposed algorithm for different test cases are portrayed. Finally, conclusion is given in section-VI.

II. Proposed Dual Role CDSC

Usually the harmonic spectrum of grid voltage in a distribution system is dominated by the lower order odd harmonics because of non-linear loads which are often connected to the grid. These harmonics of order h = -5, +7...etc., are termed as symmetric harmonics. But with steep rise in the usage of single phase non-linear load which causes unbalance and thereby leads to occurrence of asymmetric harmonics of order h = +5, -7... etc., along with triplen harmonics. In this case if any grid disturbances occur say voltage sag then it affects the DVR control algorithm in detecting the sag and thereby chances of maloperation. Thus, an effective filter is necessary to eliminate these harmonics (h=+5, +7...). In this paper CDSC based prefilter is adopted which extracts ISC of the grid voltage required for voltage sags detection and for the generation of fundamental component of reference voltage for DVR. Further when grid voltages are harmonically distorted and to regulate the load voltage harmonics an extractor is designed based on the modified CDSC strategy. This extractor generates the non-fundamental component of reference voltage and is added in 180^0 phase opposition to fundamental component (from prefilter and controller). The following part of the section deals with concept of the proposed dual role CDSC operator.

A. CDSC Pre-Filter

The harmonics present in the grid voltage retain their periodic nature even when they are transformed to synchronous reference frame. DSC technique exploits this property so that it is possible to eliminate harmonic signal by summing it with half cycle delayed version. The mathematical model of DSC operator in *dq* frame is given in (1) where n is a delay operator which delays signal by T/n. Single DSC operator is not able to eliminate all the harmonics so multiple DSC operators are cascaded to form CDSC operator which accomplish the elimination process step-by-step. In this paper the CDSC operator is implemented in αβ-frame.

$$dqDSC_n\left[v(t)\right]=\frac{1}{2}\left[v(t)+v(t-T/n)\right] \tag{1}$$

$$v_{dq}(t)=e^{-j\theta}(v_{\alpha\beta}) \tag{2}$$

$$v_{dq}(t-T/n)=e^{-j(\theta-\frac{2\pi}{n})}(v_{\alpha\beta}) \tag{3}$$

By substituting (2) and (3) in (1) the DSC operator in αβ-frame is given in (4).

$$\alpha\beta DSC_n(v_{\alpha\beta}(t))=\frac{1}{2}\left[v_{\alpha\beta}(t)+e^{j\frac{2\pi}{n}}v_{\alpha\beta}(t-T/n)\right] \tag{4}$$

Delay operators n=2,4,8,16,32 can eliminate all harmonics with h = 0, ±1, ±2, ±3, ±4... ±30 in the αβ -frame. i.e. the DC offset, all symmetrical and asymmetrical harmonics up to h = ±30. But DSC_2 operator is used to filter out the even order harmonics which are very small. Thus, in this paper only DSC_4, DSC_8, DSC_{16}, DSC_{32} are cascaded to form $CDSC_{4,8,16,32}$ prefilter. Positive sequence voltages after application of a DSC_n operator is given in (5).

$$\begin{bmatrix}v^{+}_{\alpha n}\\ v^{+}_{\beta n}\end{bmatrix}=\begin{bmatrix}v_\alpha+v_\alpha\left(t-\frac{T}{n}\right)\cos\left(\frac{2\pi}{n}\right)+v_\beta\left(t-\frac{T}{n}\right)\sin\left(\frac{2\pi}{n}\right)\\ v_\beta+v_\beta\left(t-\frac{T}{n}\right)\cos\left(\frac{2\pi}{n}\right)-v_\alpha\left(t-\frac{T}{n}\right)\sin\left(\frac{2\pi}{n}\right)\end{bmatrix} \tag{5}$$

B. Modified CDSC Extractor

The concept of harmonic extraction is based on harmonic gain i.e., a zero gain of a DSC on a harmonic signal means the DSC can eliminate the harmonic signal and on the other side

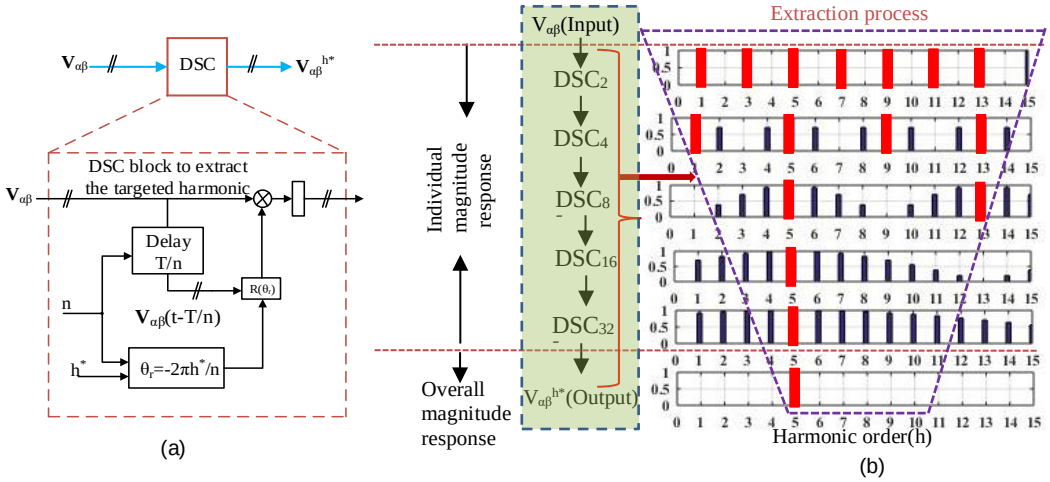

Fig.2 Dual role CDSC: (a) Extractor, (b) Individual and overall magnitude response of respective DSC and CDSC^5 operator

unity gain means the harmonic can pass through without attenuation. The modified CDSC extractor can eliminate the fundamental positive sequence signal as well to achieve the target harmonic extraction. The CDSC extractor is constructed as follows

$$DSC_n\left[v_{\alpha\beta}(t)\right]=\frac{1}{2}\left[v_{\alpha\beta}(t)+R(\theta_r).v_{\alpha\beta}(t-T/n)\right] \quad (6)$$

where R(θ_r) is given as $\begin{bmatrix}\cos\theta_r & \sin\theta_r\\ -\sin\theta_r & \cos\theta_r\end{bmatrix}$ and rotation angle $\theta_r = -2\pi h^*/n$. Fig.2(a) depicts the block diagram of (6).

For illustration purpose, let us consider a typical harmonic scenario where the voltage source consists of h=-1, ±3,5, ±7, 9, ±11, 17, ±19…. ±30. Let the target harmonic to be extracted is h^*=5 then extractor should eliminate h=±3, ±7, 9, ±11, 17, ±19…. ±30. To achieve this 5 DSC blocks of n=2(even order harmonics and DC components), n=4(-29, -25, -21, -17, -13, -9, -5, -1, 3, 7, 11, 15, 19, 23, 27, 31), n=8(-39, -31, -23, -15, -7, 1, 9, 17, 25, 33, 41) n=16(-19, -3, 13, 29) and n=32(-11, 21) are cascaded to form $CDSC^5_{2,4,8,16,32}$ extractor. Fig.2(b) depicts that the constructed $CDSC^5_{2,4,8,16,32}$ operator eliminates all undesired harmonics by providing zero gain and extracts the 5th harmonic component by providing unity gain.

C. Asymmetric Harmonics

A dynamic model has been implemented in PSCAD in order to simulate the operation of different PLL's i.e. CDSC-PLL, DSOGI-PLL, DSC-PLL, SRF-PLL and results are presented in Fig.3 under two phase sag with asymmetric grid voltage harmonics. The operation of aforementioned PLL's is demonstrated in Fig.3 (a)-(c), where it is noticed that time taken to detect frequency and phase angle is different for all PLL's. The moment when sag is created Fig.3 (b) shows that both SRF-PLL and DSC-PLL have an undershoot of more than 75% respectively. The time taken by DSC-PLL to reach the tolerance band is 5 ms but SRF-PLL oscillates above the tolerance band. Similarly, Fig.3(c) depicts DSOGI-PLL and CDSC-PLL, though both PLL's take less time to reach tolerance band but possess an undershoot of 16% and 8% respectively. Therefore CDSC-PLL is the preferable solution as it is operating accurately during asymmetric voltage sags.

There are some considerations for the practical (digital) implementation of CDSC operator. Ideally, the delay time (T/n) of DSC should correspond to an integer number of delay samples (N_n = N/n) but in practical scenario N_n is hardly an integer. So N_n should be rounded by taking the floor (N_{nf} = floor (N_n)) or the ceiling (N_{nc} = ceil (N_n)). The resulted delay buffer size becomes imprecise, and thereby causes small discretization error in the operation of DSC. Such error usually has limited effect (for small frequency variations viz., nominal frequency (f) ± 0.3 and error ≈ 0.6%). However, if the system demands higher detection accuracy (if the aforementioned range exceeds) then the CDSC technique can be further improved by adopting the linear interpolation method [27]. In this paper the results are focused on mitigation of symmetric and asymmetric voltage sags and harmonics at constant frequency thus avoiding discretization error. (N corresponds to samples f_s (sampling frequency) /f (nominal frequency).

III. DVR Control

The schematic of dual role CDSC based DVC algorithm for DVR is shown in Fig.4(a). At first CDSC- prefilter extracts ISC of the fundamental grid voltage in stationary frame. The extracted ISC is transformed to *dq*-frame and fed to controller which generates fundamental component of compensation voltage. On the other hand, an extractor based on modified CDSC strategy is designed which extracts desired harmonic components from load voltages. The harmonic extraction block generates non-fundamental component of compensation voltage and added 180^0 phase opposition with fundamental component. Finally, the resultant is fed to PWM block to produce reference voltage for compensation. It has been considered a sufficient battery energy storage system (BESS) to support the real power required by DC link capacitor of DVR. The DVC implemented in this paper is a multiloop with a voltage and inductor current as feedback signals designed in synchronous reference frame. It consists of positive and negative sequence controllers (PSC & NSC) to compensate for balanced and unbalanced voltage sags. The voltage and current feedback loops of DVC employ proportional controllers to track the reference voltages accurately. Equations of the positive controllers are given in (7) - (10) respectively.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2829678, IEEE Transactions on Industrial Electronics

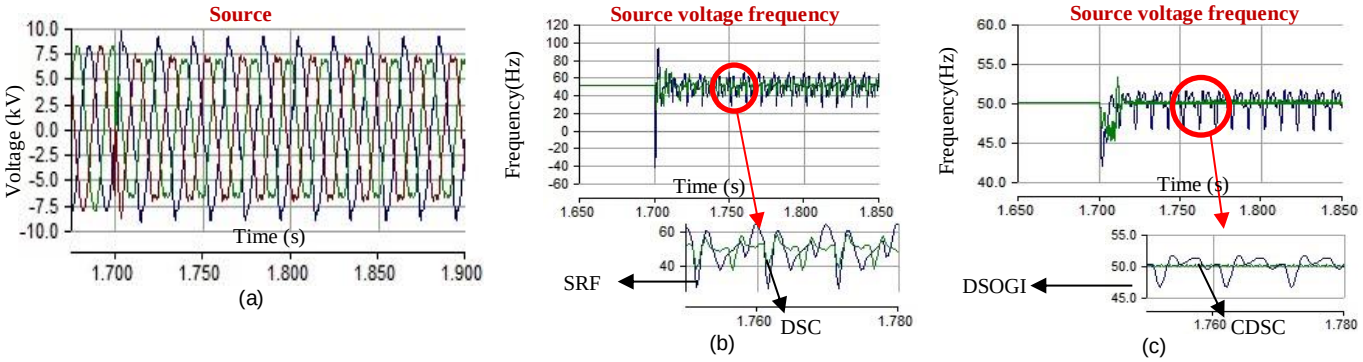

Fig.3: Simulation results for asymmetric harmonics with 20% sag in two phases: (a) Source voltage, (b) Frequency response of SRF-PLL and DSC-PLL, (c) Frequency response of DSOGI-PLL and CDSC-PLL.

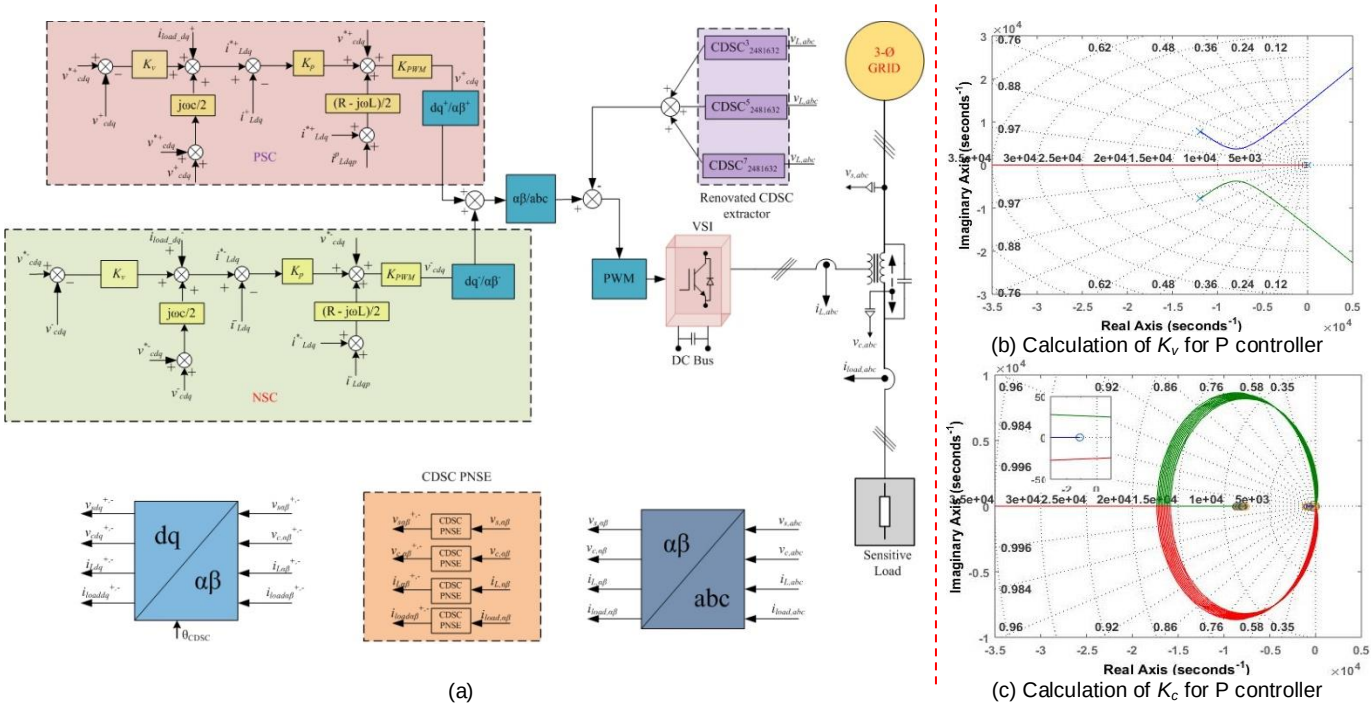

Fig. 4 Control scheme for DVR (a) Block diagram, (b) - (c) Root loci of P controller

positive controllers are given in (7) - (10) respectively.

$$i^*_{Ldp} = i_{load\_dp} - \left(\frac{\omega c_f}{2}\right)\left(v^*_{cqp} + v_{cqp}\right) + K_u\left(v^*_{cdp} - v_{cdp}\right) \quad (7)$$

$$i^*_{Lqp} = i_{load\_qp} + \left(\frac{\omega c_f}{2}\right)\left(v^*_{cdp} + v_{cdp}\right) + K_u\left(v^*_{cqp} - v_{cqp}\right) \quad (8)$$

$$v^*_{iqp} = v^*_{cqp} + R_f i_{Lqp} - \left(\frac{\omega L_f}{2}\right)\left(i^*_{Ldp} + i_{Ldp}\right) + K_p\left(i^*_{Lqp} - i_{Lqp}\right) \quad (9)$$

$$v^*_{idp} = v^*_{cdp} + R_f i_{Ldp} - \left(\frac{\omega L_f}{2}\right)\left(i^*_{Lqp} + i_{Lqp}\right) + K_p\left(i^*_{Ldp} - i_{Ldp}\right) \quad (10)$$

Where K_p, K_u are proportional gains of current and voltage loops respectively of the DVC. The positive and negative sequence controllers are shown in Fig.4(a).

A. Design of Controller Parameters

The objective of tuning the controller is to find the coefficients of proposed CDSC based DVC controller. The DVC implemented in this paper is a multiloop with a capacitor voltage and inductor current as feedback signals designed in the synchronous reference frame. It consists of Positive Sequence Controller (PSC) and Negative Sequence Controller (NSC) to compensate for balanced and unbalanced voltage sags. The voltage and current feedback loops of DVC employ proportional controllers to track the reference voltages accurately. Both PSC and NSC constitutes to 8 controllers (four with respect to PSC and four with respect to NSC). In this section the tuning of two controller gains K_v and K_c among the four controllers of PSC are discussed. K_v refers to outer loop voltage controller gain, and K_c refers to inner loop current controller gain (PSC). An extended Root Locus Design (RLD) [27] method is adopted to tune the controller coefficients. Fig. 4(b), (c) shows the extended RLD for tuning the coefficients of P controller. Firstly, to tune the value of K_c, the root locus for K_c is drawn as shown in Fig. 4(c) for all the values of K_v varied stepwise from its minimum stable value to maximum stable value obtained by Routh Hurwitz (RH) stability criterion. Based

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2829678, IEEE Transactions on Industrial Electronics

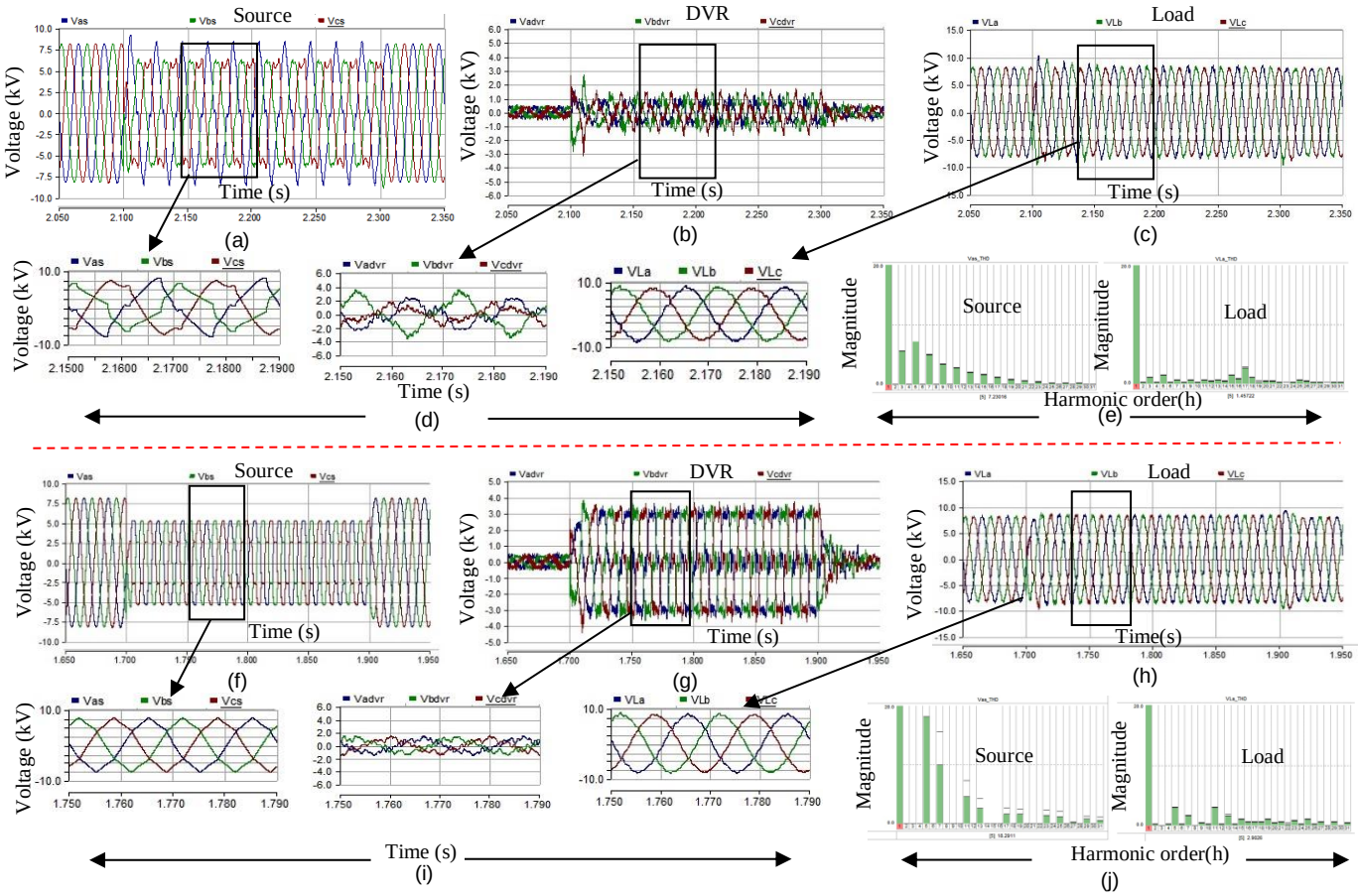

Fig. 5. Testing of DVR response during (a)-(c) Two phase sag with asymmetric odd order harmonics (d), (e) Zoomed view & harmonic spectra under asymmetric harmonics (f) – (h) Three phase balanced sag with symmetric odd order harmonics (i),(j) Zoomed view and harmonic spectra under symmetric harmonics

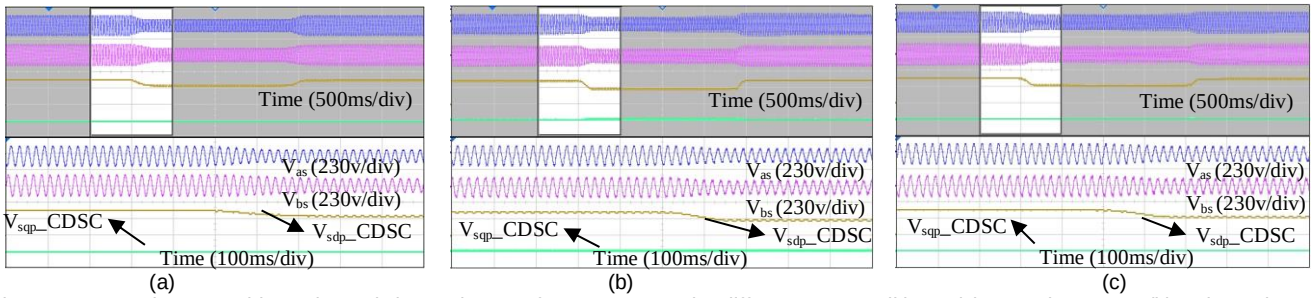

Fig. 6. Source voltages and its estimated dq_{sp}- voltages of CDSC-PLL under different test conditions: (a) Two phase sag, (b) Balanced sag with symmetric harmonics, (c) Balanced sag under asymmetric harmonics.

on maximum relative stability the optimal value of K_c is obtained. From the obtained value of K_c (Fig. 4(c)) the root locus is plotted for transfer function having gain K_v as shown in Fig.4(b) and its value is calculated based on relative stability. To design the controller with high robustness, relative stability is considered for optimum tuning of controller parameters. It is essential that load voltage tracking accuracy should be sustained during voltage sags. Thus, the controller parameters are tuned to address all the above requirement. The same procedure is followed to tune the other controller gains.

IV. Simulation Results

A PSCAD/EMTDC model of a three phase DVR with the proposed control scheme is built and its performance is validated for asymmetric & symmetric voltage sags and harmonics, but results are presented for harmonics case. The parameters of the 10 kV distribution system with DVR installed between source and load which are considered for simulation studies are provided in Appendix [3].

A. Performance of DVR under Asymmetric & Symmetric harmonics condition

The use of single phase non-linear loads could generate asymmetric odd voltage harmonics such as n = +5, -7... Hence by connecting unbalanced non-linear loads asymmetric odd harmonics are generated at the PCC. Under such non-linear loads, phase-a voltage contains third harmonic of 5.53%, fifth harmonic of 7.23% as shown in Fig.5 (e). Further the terminal voltages have a total harmonic distortion of 13.07%. Fig.5 (a) depicts the supply voltages with a two-phase voltage dip of 20%. CDSC pre-filter extracts the ISC accurately even under asymmetric harmonics. Positive and negative sequence

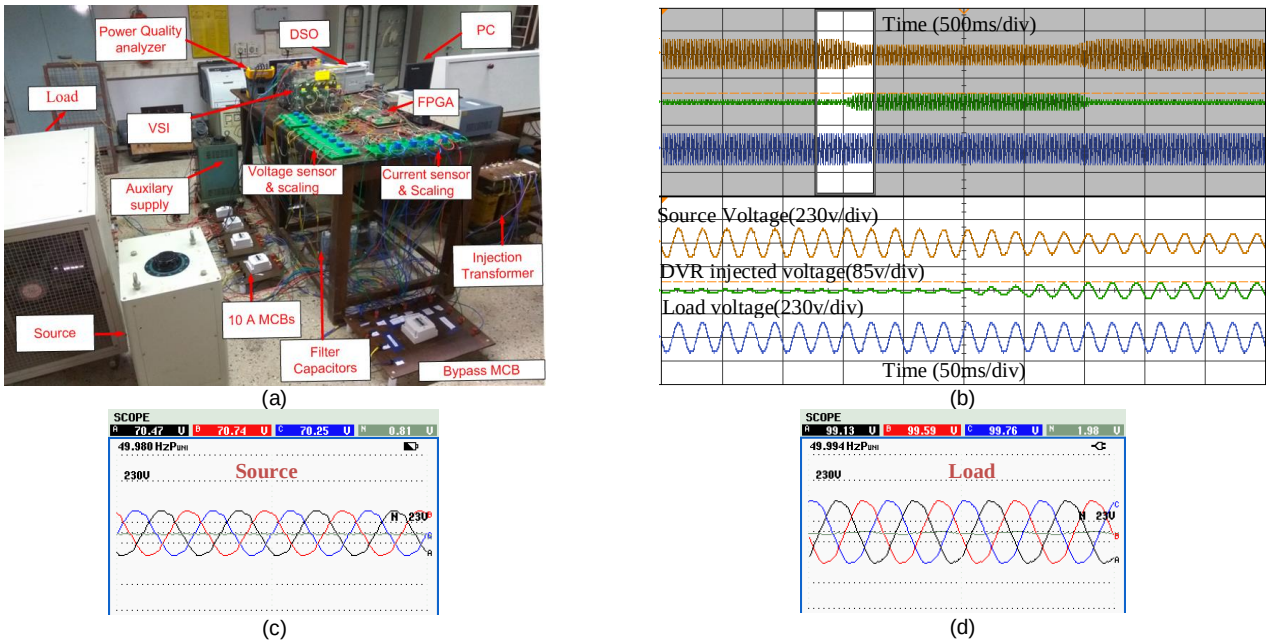

Fig.7. Expreimental results: (a) Experimental setup of laboratory prototype, (b) Dynamic response of DVR under symmetric sag, (c)-(d) Steady state voltage waveform of source and load under symmetric sag.

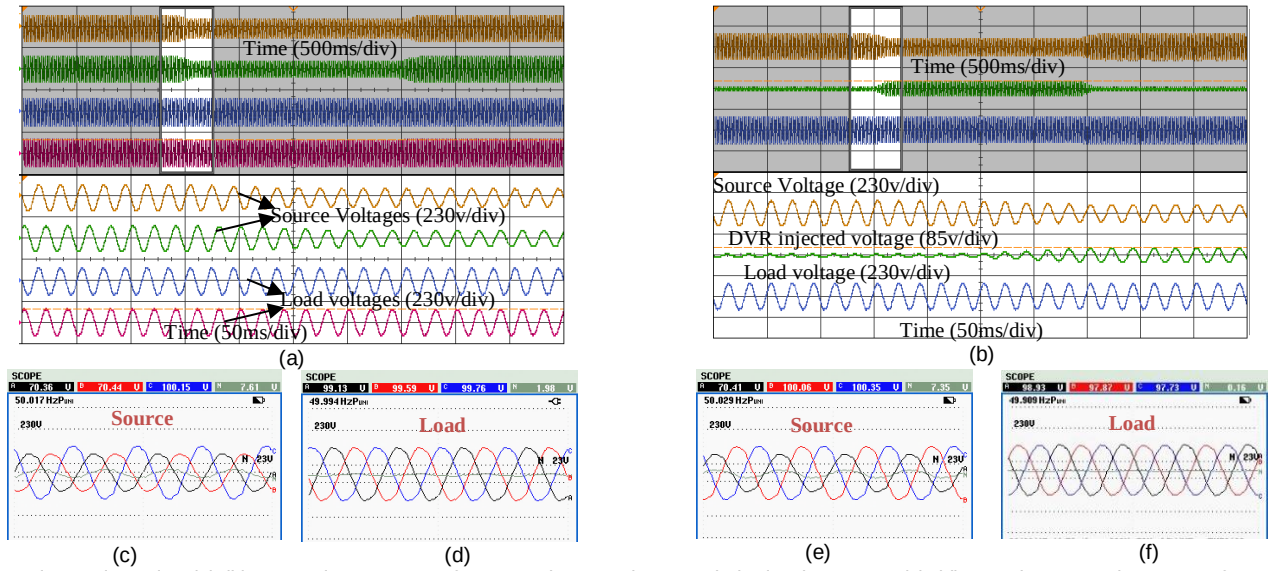

Fig.8. Expreimental results: (a),(b) Dynamic response of DVR under two phase and single phase sag, (c)-(d) Steady state voltage waveform of source and load under two phase sag, (e)-(f) Steady state voltage waveform of source and load under single phase sag,

controllers compensate for the voltage sag and restore the fundamental of load voltage to nominal value as seen in Fig.5 (c). The effectiveness of the modified CDSC based extractor under asymmetric harmonics can be verified from the load THD waveform from Fig.5(e) where it is observed that the third and fifth harmonics are restricted to 0.99%, 1.45% respectively. After harmonic compensation by dual role CDSC based DVC, the load voltages have a THD of 3.7%. The DVR injected voltages are shown in Fig.5 (b) and zoomed view of source, DVR injected, and load voltages are presented in Fig.5 (d). Fig.5 (f)-(j) shows the DVR performance during the presence of symmetric harmonics in source voltage. The THD waveform shows the efficacy of control algorithm where load voltage THD is reduced to 3.89% from source voltage THD of 21.4% as depicted in Fig.5 (j). Fig.5 (i) represents the zoomed part of source, DVR and load voltages under symmetric harmonics case.

V. Experimental results

A 100 V, 0.5 kVA scaled down DVR prototype is developed in laboratory to conduct experimental studies. Hardware configuration of the DVR prototype consists of a SEMIKRON – made VSI, Fluke 435 power quality analyzer and a resistive load as shown in Fig. 7(a). The DC link of the VSI is powered by an auxiliary supply as shown in Fig.7(a). The control platform is based on Altera cyclone-II FPGA controller using Quartus GUI. The FPGA board is interfaced with EEPROM (configuration device), physical interfacing devices viz., ADC,

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2829678, IEEE Transactions on Industrial Electronics

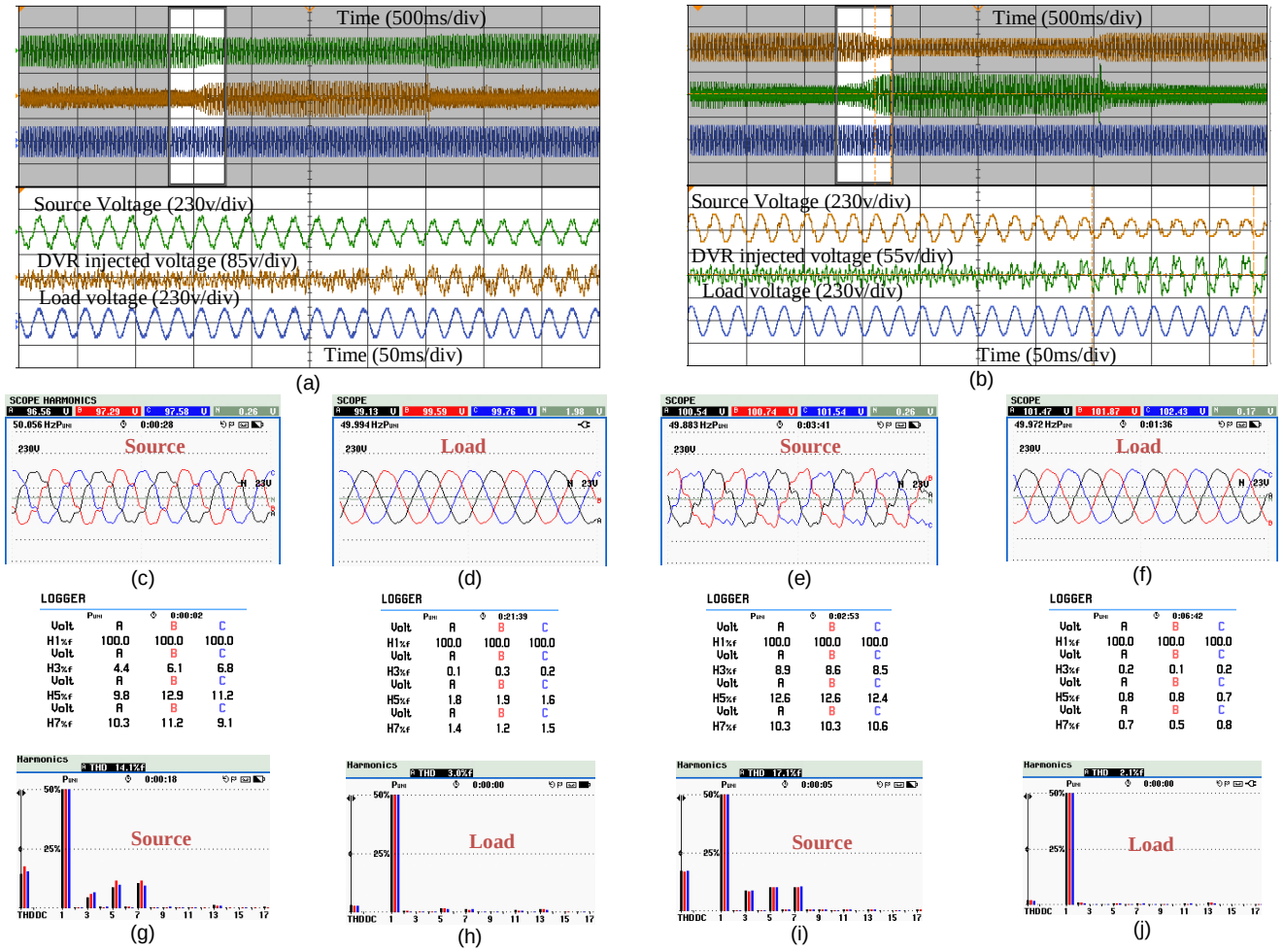

Fig.9. Experimental results. (a)-(b) Dynamic reponse of DVR under balanced sag with asymmetric and symmetric harmonics, (c)-(f) steady state voltage waveform of source and load under asymmetric and symmetric harmonics, (g)-(h) Harmonic spectrum of source and load voltages during asymmetric harmonics, (i)-(j) Harmonic spectrum of source and load voltages during symmetric harmonics.

DAC, Digital I/O's, USB device and synchronous Dual-PORT SRAM (CY7C09389V). Analog signals are converted to digital form using 12-bit 4-channel bipolar ADCs(AD7864) and the signals are interfaced to FPGA. The scaling circuits provide necessary scaling of measured values to interface with the FPGA board. The system parameters are listed in Table 2. The experimental studies are conducted for symmetrical and asymmetrical voltage sags, harmonics respectively and their results are presented.

B. Performance of CDSC-PLL under Distorted Grid Conditions

In simulation studies, it is found that CDSC – prefilter performs better during the distorted grid conditions. Hence CDSC-PLL algorithm is implemented in FPGA board. It is tested for two phase sag, symmetric and asymmetric grid voltage harmonics.

1) Performance of CDSC-PLL under Two phase sag:

The CDSC-PLL algorithm is subjected to two phase sag to test its ability in eliminating negative sequence voltages. During sag condition, the negative sequence components present in the grid voltage leads to oscillating double frequency components in *dq*-frame but Fig.6(a) shows CDSC prefilter cancel out oscillating component to keep V_{sdq} ripple free.

2) Performance of CDSC-PLL under Asymmetric and Symmetric harmonics

A balanced dip of 30% is generated in phase-a and phase-b of the supply voltage with symmetric and asymmetric harmonics respectively. The absence of ripple in V_{sdq} of CDSC-PLL shown in Fig.6 (b), (c) indicates the effectiveness of its prefilter in eliminating harmonics.

B. *Balanced Sag*

The laboratory prototype DVR is connected to a load of 0.5 kW for the following experimental cases. A three-phase voltage dip of 30% is initiated by using a three- phase auto transformer for a duration of 840 ms which can be observed from supply voltage waveform shown in Fig. 7(b), (c). DVR mitigates the voltage sag and restores the load voltage to a constant value as shown in Fig. 7(d). DVR injected voltages can be observed in Fig. 7(b).

C. Two Phase Sag

Three single phase transformers are employed to create unbalanced voltage sag by reducing the voltage in phase-a and phase-b respectively by 30% as shown in Fig.8(a), (c). DVR compensates for both negative and positive sequence voltage and maintains a constant voltage waveform of phase-a and

phase-b as depicted in Fig.8(a), (d). DVR injected voltages are shown in Fig.8 (a).

D. Single Phase Sag

The dynamic response of a DVR for a 30% dip in phase-a is portrayed in Fig. 8(b). The supply voltage drops to 70V in phase-a as shown in Fig.8(e). The control algorithm responds immediately after detection of sag and injects voltage as seen in Fig. 8(b), (f) to keep the load voltage unchanged.

E. Asymmetric Harmonics

To evaluate the performance of DVR with harmonics in voltage source a non – linear load of diode rectifier type is connected in parallel feeder line as shown in Fig.1. The steady state grid voltage is distorted by harmonics due to the addition of nonlinear loads and is shown in Fig.9 (a), (c). Along with odd harmonics, a balanced voltage dip of 30% is also generated to test the performance of control algorithm. In this case the, CDSC prefilter and controller (PSC & NSC) tracks the fundamental component of reference voltages and modified CDSC extractor extracts the respective harmonics present in the load voltage and generates non-fundamental component which is added in 180^0 phase opposition with the fundamental component. It can be seen from Fig.9 (a) where zoomed part of rectangular portion clearly shows that the load voltage is maintained constant during sag and also harmonics are mitigated. The reduction in THD is reflected from Fig.9(g), (h) where THD of source voltage is 14.1% and respective load voltage is 3.0%.

F. Symmetric Harmonics

In this case the performance of dual role CDSC based DVC is tested by connecting unbalanced non-linear loads at the PCC to generate odd symmetric harmonics. The harmonic contents introduce a THD of 17.1% in grid voltage as shown in Fig.9 (i) along with a balanced voltage dip of 30% which can be observed from Fig.9 (b). CDSC pre-filter extracts the ISC accurately even under symmetric harmonics. DVC algorithm compensates for the voltage sag and restores fundamental of load voltage to the nominal value as seen in Fig.9(b), (f). The THD of the total voltage is reduced to 2.1% which is evident from Fig.9(j).

V. Conclusion

This paper presents the flexible control strategy for the effective control of DVR. It is based on the CDSC operator which plays dual role as a prefilter and as an extractor. Therefore, the main contribution of this paper is development of dual role CDSC based DVC algorithm for compensating voltage sags and simultaneously mitigating the harmonics from load voltage. Firstly, the ISC of the grid voltages are obtained using a CDSC pre-filter, which is customized to filter out symmetric and asymmetric voltage harmonics. Then CDSC based DVC algorithm with positive and negative sequence controllers is implemented in *dq*-frame to track the DVR reference voltages. Further the load voltage THD is reduced to 3.0% (from 14.1%) in asymmetric harmonic case and to 2.1% (from 17.1%) in symmetric harmonics case by adding an extractor based on modified CDSC strategy to the control algorithm which is designed to extract the dominant lower order harmonics from the load voltage. In summary, based on the simulation studies and experimental results the proposed algorithm operates effectively even when the grid voltage is distorted with variations such as balanced, unbalanced sags, and during the presence of asymmetric and symmetric voltage harmonics.

Appendix

Table-I
Experimental setup –System parameters

Device	Description	Value
Source	AC voltage (phase voltage rms)	100 V
	Frequency	50 Hz
Load (Star)	Resistance	0-400 Ω , 5A
Inverter	Switching frequency	5 kHz
	DC link Voltage	200 V
Filter	Capacitance	70 μF
Injection Transformer	Inductance, Turns ratio	720 μH, 1:1
	Primary and secondary voltage	230 V

Table-II
Simulation studies –System parameters

Device	Description	Value
Supply	AC voltage (LL rms)	10 kV
	Frequency	50 Hz
	Supply impedance (Z_s)	2.6 Ω, 0.006048 mH
Load (Delta)		45 kW/6670 Ω
Inverter	Switching frequency	5 kHz
	DC link Voltage	600 V
Filter	Inductance (L_f)	260 μH
	Capacitance (C_f)	120 μF
Injection Transformer (per phase)	Rated Power (S_{tra})	67 kVA
	Primary Voltage (V_1) (LL)	2900 V
	Secondary voltage(V_2)	290 V

Acknowledgment

This work was supported by the administration of the National Institute of Technology Karnataka , Surathkal and the Department of Science and Technology, India, under Project Grant SB/FTB/ETA-0020/2014.

References

[1] J. G. Nielsen and F. Blaabjerg, "A detailed comparison of system topologies for dynamic voltage restorers," in *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1272-1280, Sept.-Oct. 2005.

[2] A. Massoud, S. Ahmed, P. Enjeti, and B. Williams, "Evaluation of a multilevel cascaded-type dynamic voltage restorer employing discontinuous space vector modulation," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2398–2410, Jul. 2010.

[3] J. G. Nielsen, "Design and Control of a Dynamic Voltage Restorer," Ph.D. dissertation, Inst. Energy Technol., Aalborg Univ., Aalborg, Denmark, 2002.

[4] H. Awad, H. Nelsen, F. Blaabjerg and M. J. Newman, "Operation of static series compensator under distorted utility conditions," in *IEEE Transactions on Power Systems*, vol. 20, no. 1, pp. 448-457, Feb. 2005.

[5] H. Awad, J. Svensson and M. Bollen, "Mitigation of unbalanced voltage dips using static series compensator," in *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 837-846, May 2004.

[6] E. Ebrahimzadeh, S. Farhangi, H. Iman-Eini, F. Badrkhani Ajaei and R. Iravani, "Improved Phasor Estimation Method for Dynamic Voltage Restorer Applications," in *IEEE Transactions on Power Delivery*, vol. 30, no. 3, pp. 1467-1477, June 2015.

[7] G. Chen, L. Zhang, R. Wang, L. Zhang and X. Cai, "A Novel SPLL and Voltage Sag Detection Based on LES Filters and Improved Instantaneous Symmetrical Components Method," in *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1177-1188, March 2015.

[8] S. Golestan, M. Ramezani, J. M. Guerrero and M. Monfared, "dq-Frame Cascaded Delayed Signal Cancellation- Based PLL: Analysis, Design, and Comparison With Moving Average Filter-Based PLL," in *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1618-1632, March 2015.

[9] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A New Single-Phase PLL Structure Based on Second Order Generalized Integrator," in 37th IEEE Power Electronics Specialists Conference, pp. 1–6, June 2006.

[10] Y. F. Wang and Y. Wei Li, "Analysis and Digital Implementation of Cascaded Delayed-Signal-Cancellation PLL," in *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1067-1080, April 2011.

[11] Y. F. Wang and Y. W. Li, "Grid Synchronization PLL Based on Cascaded Delayed Signal Cancellation," in *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1987-1997, July 2011.

[12] F. A. S. Neves, M. C. Cavalcanti, H. E. P. de Souza, F. Bradaschia, E. J. Bueno and M. Rizo, "A Generalized Delayed Signal Cancellation Method for Detecting Fundamental-Frequency Positive-Sequence Three-Phase Signals," in *IEEE Transactions on Power Delivery*, vol. 25, no. 3, pp. 1816-1825, July 2010.

[13] S. S. Choi, J. D. Li and D. M. Vilathgamuwa, "A generalized voltage compensation strategy for mitigating the impacts of voltage sags/swells," in *IEEE Transactions on Power Delivery*, vol. 20, no. 3, pp. 2289-2297, July 2005.

[14] Y. W. Li, D. M. Vilathgamuwa, F. Blaabjerg and P. C. Loh, "A Robust Control Scheme for Medium-Voltage-Level DVR Implementation," in *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 2249-2261, Aug. 2007.

[15] H. K. Al-Hadidi, A. M. Gole and D. A. Jacobson, "A Novel Configuration for a Cascade Inverter-Based Dynamic Voltage Restorer With Reduced Energy Storage Requirements," in *IEEE Transactions on Power Delivery*, vol. 23, no. 2, pp. 881-888, April 2008.

[16] E. Babaei, M. F. Kangarlu and M. Sabahi, "Dynamic voltage restorer based on multilevel inverter with adjustable dc-link voltage," in *IET Power Electronics*, vol. 7, no. 3, pp. 576-590, March 2014.

[17] D. M. Vilathgamuwa, A. A. D. R. Perera and S. S. Choi, "Voltage sag compensation with energy optimized dynamic voltage restorer," in *IEEE Transactions on Power Delivery*, vol. 18, no. 3, pp. 928-936, July 2003.

[18] A. M. Rauf and V. Khadkikar, "An Enhanced Voltage Sag Compensation Scheme for Dynamic Voltage Restorer," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 2683-2692, May 2015.

[19] Barros, J. Dionísio, and J. Fernando Silva, "Multilevel optimal predictive dynamic voltage restorer," in *IEEE Transactions on Industrial Electronics*, vol. 57, no.8, pp. 2747-2760, August 2010.

[20] W. Guo, L. Xiao, S. Dai and L. Lin, "Control Strategy of a 0.5 MVA/1 MJ SMES Based Dynamic Voltage Restorer," in *IEEE Transactions on Applied Superconductivity*, vol. 20, no. 3, pp. 1329-1333, June 2010.

[21] J. G. Nielsen, F. Blaabjerg and N. Mohan, "Control strategies for dynamic voltage restorer compensating voltage sags with phase jump," *Applied Power Electronics Conference and Exposition, 2001. APEC 2001. Sixteenth Annual IEEE*, Anaheim, CA, pp. 1267-1273 vol.2, 2001.

[22] J. Roldán-Pérez, A. García-Cerrada, J. L. Zamora-Macho, P. Roncero-Sánchez, and E. Acha, "Troubleshooting a digital repetitive controller for a versatile dynamic voltage restorer," *International Journal of Electrical Power and Energy Systems*, vol. 57. pp. 105–115, 2014.

[23] G. Chen, M. Zhu and X. Cai, "Medium-voltage level dynamic voltage restorer compensation strategy by positive and negative sequence extractions in multiple reference frames," in *IET Power Electronics*, vol. 7, no. 7, pp. 1747-1758, July 2014.

[24] M. İnci, K. Ç. Bayındır, and M. Tümay, "Improved Synchronous Reference Frame based controller method for multifunctional compensation," *Electric Power Systems Research*, vol. 141. 2016.

[25] M. J. Newman, D. G. Holmes, J. G. Nielsen and F. Blaabjerg, "A dynamic voltage restorer (DVR) with selective harmonic compensation at medium voltage level," in *IEEE Transactions on Industry Applications*, vol. 41, no. 6, pp. 1744-1753, Nov.-Dec. 2005.

[26] Li, Peng, Lili Xie, Jiawei Han, Shilin Pang, and Peihao Li, "New Decentralized Control Scheme for Dynamic Voltage Restorer Based on the Elliptical Trajectory Compensation," in *IEEE Transactions on Industrial Electronics*, vol.64, no.8, pp.6484-6495, August 2017

[27] Y. F. Wang and Y. Wei Li, "Analysis and Digital Implementation of Cascaded Delayed-Signal-Cancellation PLL," in *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1067-1080, April 2011.

[28] Minhee Kwon, Hyuk-Jun, "Extended root-locus technique applied to pole placenment for PI Controller Design," *in Proc.11th Int.Conf. on control (CONTROL), UKACC.*, Aug 2016.

A. Karthikeyan received the B.E. degree in Electrical Engineering from Bharathidasan University, India in 2002, the M.S. (by research) and Ph.D. degrees from National Institute of Technology, Tiruchirappalli, India, in 2008 and 2013 respectively in Electrical Engineering. presently, he is Assistant Professor with the Department of Electrical and Electronics Engineering, National Institute of Technology, Surathkal, India. His research interests include control of power converter in drives, renewable energy systems and power conditioning.

D. G. Abhilash Krishna received the B. Tech degree in Electrical and Electronics Engineering from Jawaharlal Nehru Technological University, Anantapur, India in 2013, the Master's degree in Power Electronics and Drives from Vellore Institute of Technology University, Vellore, India, in 2015. He is presently working toward the Ph.D. degree in Department of Electrical and Electronics Engineering at National Institute of Technology, Surathkal, India. His current research interests include control of power converters and power quality.

Sushant Kumar received the B.Tech degree in Electrical and Electronics Engineering from WBUT, West Bengal, India in 2014, the Master's degree in Power and Energy Systems from National Institute of Technology, Surathkal, India, in 2017. Presently he is working as site engineer in RVNL, Delhi, India.

B. Venkatesa Perumal received B.E degree in 1991 from Madras University in Electrical Engineering, M.E. degree in Power Electronics and Drives from Bharathidasan University, India, in 2001, and Ph.D. degree in electrical engineering from Indian Institute of Technology Delhi, New Delhi, India, in 2007. Previously he worked for GE, Schneider electric, as technical leader for Power Electronic R&D Division, SunEdison, Bangalore, India. Presently, he is Associate Professor and Head of the Department of Electrical and Electronics Engineering, National Institute of Technology, Surathkal, India. His research interests include applications of power electronics in health care, solar generation and brushless generation.

S. Mishra is a Professor with the Department of Electrical Engineering, Indian Institute of Technology Delhi, India. Dr. Mishra has been honored with many prestigious awards such as the INSA Young Scientist Medal in 2002, the INAE Young Engineers Award in 2002, and recognition as the DST Young Scientist in 2001 to 2002, etc. He is a Fellow of The National Academy of Sciences India, Indian National Academy of Engineering, Institute of Engineering and Technology (IET), London, U.K., and Institute of Electronics and Communication Engineering (IETE), India.